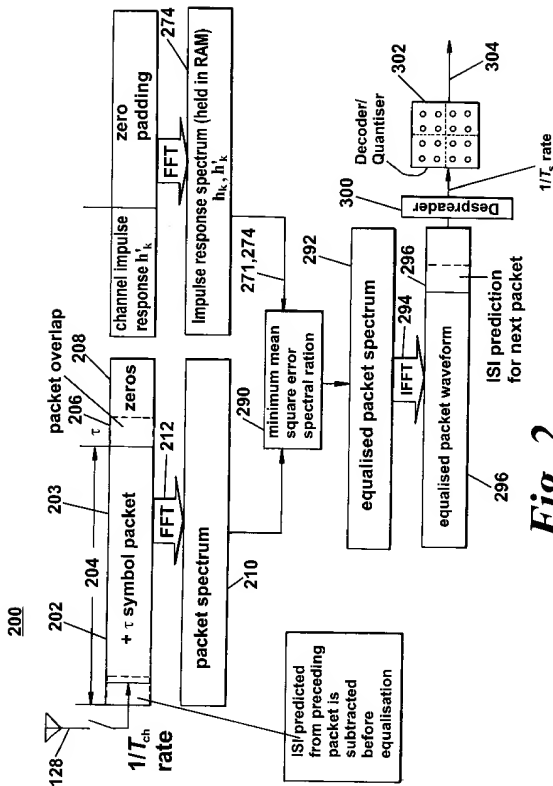


Fig. 1
(PRIOR ART)



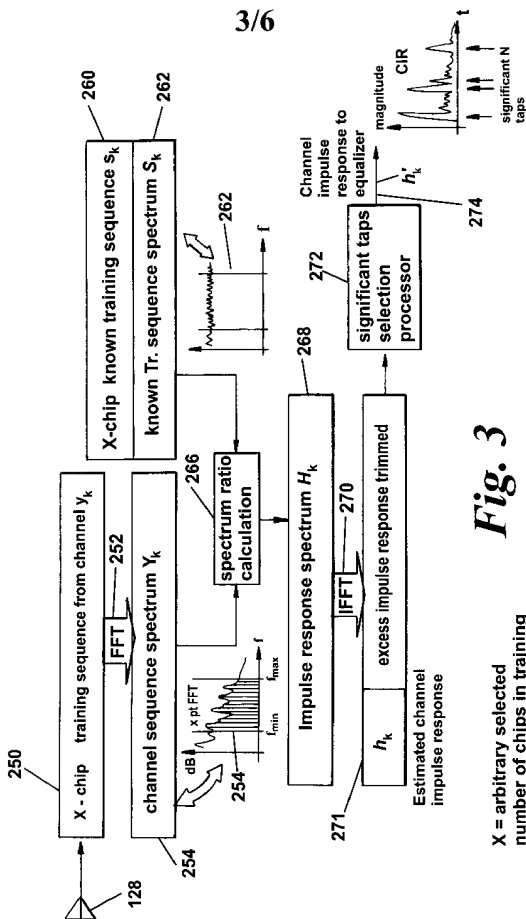
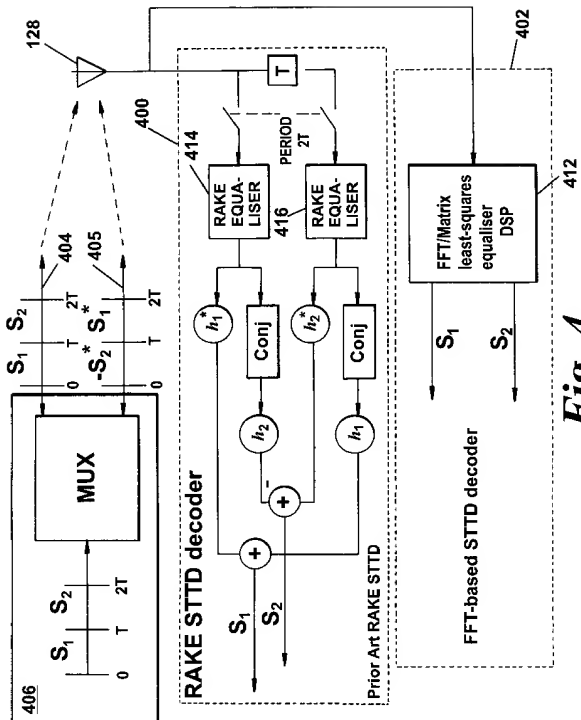


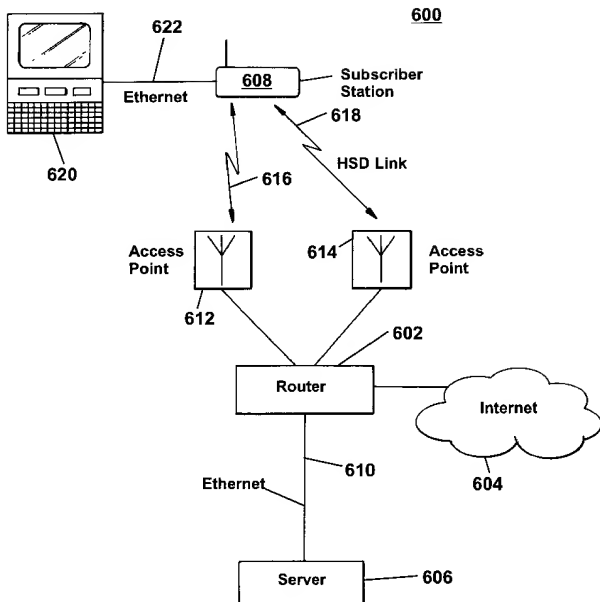
Fig. 3

X = arbitrary selected
number of chips in training
sequence set by system standard



$h_1'(0) + 0$	$0 - h_2'(0)$	$-h_1'(0) + 0$	$0 - h_2'(0)$	0
$h_1'(1) + h_2'(0)$	$h_1'(0) - h_2'(1)$	$-h_1'(1) + h_2'(0)$	$-h_1'(0) - h_2'(1)$	0
$h_1'(0) + 0$	$0 - h_2'(0)$	$h_1'(0) - 0$	$0 + h_2'(0)$	0
$h_1'(1) + h_2'(0)$	$h_1'(0) - h_2'(1)$	$h_1'(1) - h_2'(0)$	$h_1'(0) + h_2'(1)$	0
$h_1'(2) + h_2'(1)$	$h_1'(1) - h_2'(2)$	$-h_1'(2) + h_2'(1)$	$-h_1'(1) - h_2'(2)$	0
$h_1'(3) + h_2'(2)$	$h_1'(2) - h_2'(3)$	$-h_1'(3) + h_2'(2)$	$-h_1'(2) - h_2'(3)$	0
$h_1'(2) + h_2'(1)$	$h_1'(1) - h_2'(2)$	$h_1'(2) - h_2'(1)$	$h_1'(1) + h_2'(2)$	0
$h_1'(3) + h_2'(2)$	$h_1'(2) - h_2'(3)$	$h_1'(3) - h_2'(2)$	$h_1'(2) + h_2'(3)$	0
$h_1'(4) + h_2'(3)$	$h_1'(3) - h_2'(4)$	$-h_1'(4) + h_2'(3)$	$-h_1'(3) - h_2'(4)$	0
$h_1'(5) + h_2'(4)$	$h_1'(4) - h_2'(5)$	$-h_1'(5) + h_2'(4)$	$-h_1'(4) - h_2'(5)$	0
$h_1'(4) + h_2'(3)$	$h_1'(3) - h_2'(4)$	$h_1'(4) - h_2'(3)$	$h_1'(3) + h_2'(4)$	0
$h_1'(5) + h_2'(4)$	$h_1'(4) - h_2'(5)$	$h_1'(5) - h_2'(4)$	$h_1'(4) + h_2'(5)$	0
....

Layout of channel impulse responses in \tilde{c} *Fig. 5*

**Fig. 6**